IN THE CLAIMS

What is claimed is:

1. An apparatus for comparing numbers comprising:

a redundant arithmetic circuit having a capacity to receive a plurality of comparison operands, each comparison operand representing a value of a first set of values, the redundant arithmetic circuit further having a capacity to receive a first operand of the plurality of comparison operands in a first redundant form; and

comparison logic coupled with the redundant arithmetic circuit to generate a comparison result with respect to the first operand represented in the first redundant form and at least one other operand of the plurality of comparison operands.

2. The apparatus recited in claim 1 wherein each value of the first set of values is representable by said first operand and wherein each value of the first set of values is representable by said at least one other operand.

3. The apparatus recited in claim 1 wherein the comparison logic generates the comparison result indicating the comparison is true when the first

operand is greater than the at least one other operand of the plurality of comparison operands.

4. The apparatus recited in claim 1 wherein the comparison logic generates the comparison result indicating the comparison is true when the first operand is less than the at least one other operand of the plurality of comparison operands.

5. The apparatus recited in claim 1 wherein the comparison logic generates the comparison result indicating the comparison is true when the first operand is not less than the at least one other operand of the plurality of comparison operands.

6. The apparatus recited in claim 1 wherein the redundant arithmetic circuit is to perform a subtraction operation on the plurality of comparison operands and to generate a valid first result of a subtraction operation, the first result represented in a second redundant form.

7. The apparatus recited in claim 6 further comprising:

conversion logic to produce a most significant binary digit (MSB) of the first operand represented in the first redundant form.

8. The apparatus recited in claim 7 wherein the comparison logic comprises Z-comparison logic to compare the first result to a zero represented in the second redundant form and to generate a zero result indicating that the first result is equal to zero.

9. The apparatus recited in claim 8 wherein the comparison logic generates the comparison result indicating the comparison is true responsive to the MSB and the zero result.

10. The apparatus recited in claim 8 wherein the comparison logic generates the comparison result indicating the comparison is true when the first operand is equal to the at least one other operand of the plurality of comparison operands.

11. The apparatus recited in claim 1 wherein the first set of values is a set of 2^n distinct values, each value corresponding to a distinct n-bit binary representation.

12. The apparatus recited in claim 11 wherein the first set of values is selected from the group consisting of: the set $[-2^{n-1}, 2^{n-1}-1]$ corresponding to

signed n-bit two's complement representations, and the set [0, 2^n–1] corresponding to unsigned n-bit representations.

13. The apparatus recited in claim 10 wherein the first operand of the plurality of comparison operands is represented by 2n bits in the first redundant form.

14. An apparatus for comparing numbers comprising:

an interface to receive a plurality of operands of a first set of representable values wherein the interface has the capacity to receive a first operand of the plurality of operands in a first redundant form;

a redundant arithmetic circuit to perform a subtraction operation on the plurality of operands, said arithmetic circuit to generate a valid first result of a subtraction operation, the first result represented in a second redundant form;

conversion logic coupled with the interface to produce a most significant bit of a two's complement representation from the first redundant form of the first operand;

comparison logic coupled with the arithmetic circuit and the conversion logic to generate a second result indicating the truth of a magnitude comparison operation of the first operand represented in the first redundant form with at least one other operand of the plurality of operands.

15. The apparatus recited in claim 14 wherein each of the plurality of operands can represent any value of the first set of representable values.

16. The apparatus recited in claim 14 wherein said comparison logic generates the second result indicating the truth of a magnitude comparison operation when the first operand is greater than the at least one other operand of the plurality of operands.

17. The apparatus recited in claim 14 wherein said apparatus further comprises:

Z-comparison logic coupled with the redundant arithmetic circuit to compare the first result to a zero represented in the second redundant form and to produce a zero result indicating that the first result is equal to zero.

18. The apparatus recited in claim 17 wherein the comparison logic generates the second result indicating the truth of the magnitude comparison responsive to the most significant bit produced by the conversion logic and the zero result produced by the Z-comparison logic.

19. The apparatus recited in claim 18 wherein the comparison logic generates the second result indicating the magnitude comparison is true when the first operand is less than the at least one other operand of the plurality of operands.

20. A method comprising:

receiving an operand in a first redundant form;

subtracting the operand and producing a first result in a second redundant form;

generating a zero indicator by comparing the first result to zero represented in the second redundant form;

generating a most significant binary digit (MSB) from the first redundant form of the operand; and

producing a second result of a magnitude comparison responsive to the MSB and the zero indicator.

21. The method recited in claim 20 further comprising:

generating a carry-out of the subtraction operation; and

producing the second result of the magnitude comparison responsive to the most significant bit, the carry out and the zero indicator.

22. An article of manufacture comprising:

a machine accessible medium including data that when accessed by a machine causes the machine to

receive an operand in a first redundant form,

subtract the operand in the first redundant form to produce a first result in a second redundant form, and

produce a second result of a magnitude comparison responsive to the first result in a second redundant form.

23. The article of manufacture recited in claim 22 wherein the machine accessible medium including data that when accessed by a machine further causes the machine to

generate a zero indicator by comparing the first result to zero represented in the second redundant form,

generate a most significant bit from the first redundant form of the operand,

generate a carry-out of the subtraction operation, and

produce the second result of the magnitude comparison responsive to the most significant bit, the carry out and the zero indicator.

24. An apparatus comprising:

a first switching device having a first activation input, the first switching device coupled with a first voltage terminal and a first charge accumulation node to conduct a current between the first voltage terminal and the charge accumulation node responsive to a second voltage level being applied to the first activation input;

a first discharge circuit having a first interface to receive a first plurality of signals comprising a not-zero signal, a carry-out signal, a same signal, and a signed signal, the first discharge circuit coupled with a second voltage terminal and the first charge accumulation node to conduct a current between the second voltage terminal and the charge accumulation node responsive to the not-zero signal, the carry-out signal, the same signal, and the signed signal;

a second discharge circuit having a second interface to receive a second plurality of signals comprising a not-same signal, a MSB signal, and the signed signal, the second discharge circuit coupled with the second voltage terminal and the first charge accumulation node to conduct a current between the second voltage terminal and the charge accumulation node responsive to the not-same signal, the MSB signal, and the signed signal; and

a third discharge circuit having a third interface to receive a third plurality of signals comprising the not-zero signal, the carry-out signal, and a not-signed signal, the third discharge circuit coupled with the second voltage terminal and the first charge accumulation node to conduct a current between the second

voltage terminal and the charge accumulation node responsive to the not-zero signal, the carry-out signal, and a not-signed signal.

25. An apparatus comprising:

a first comparison logic to receive a number represented in a redundant form having a plurality of digits ranked sequentially according to significance, the comparison logic comprising a plurality of digit comparison circuits each digit comparison circuit to receive signals from at most three digits of the plurality of digits and generate a digit-indication of whether a middle ranking digit of the at most three digits is zero, the comparison logic further to combine the digit-indications generated by the plurality of digit comparison circuits to generate a zero-indication of whether the number represented in redundant form is zero.

26. The apparatus recited in claim 25 further comprising:

a first carry logic to propagate a carry signal from the plurality of digits ranked sequentially according to significance to generate a carry-out.

27. The apparatus recited in claim 26 further comprising:

a second comparison logic to combine the zero-indication generated by the first comparison logic with the carry-out generated by the first carry logic to

generate a magnitude-indication of whether the number represented in redundant form is in a relation to zero selected from the group consisting of less-than zero, greater-than zero, less-than-or-equal to zero, and greater-than-or-equal to zero.

28. The apparatus recited in claim 27 further comprising:

a redundant arithmetic circuit to receive a first comparison operand and a second comparison operand and to generate the number represented in redundant form as a valid result of a subtraction operation between the first comparison operand and the second comparison operand.

29. The apparatus recited in claim 28 further comprising:

a third comparison logic to receive a first most significant binary digit (MSB) corresponding to the first comparison operand and a second MSB corresponding to the second comparison operand, the third comparison logic to generate a same-indication of whether the first MSB and the second MSB are equal, wherein the second comparison logic further combines the same-indication with the zero-indication generated by the first comparison logic and the carry-out generated by the first carry logic to generate the magnitude-indication.

30. The apparatus recited in claim 29 further comprising:

a second carry logic to generate a second carry signal from the second comparison operand; and

a conversion logic to receive the second carry signal and to generate the second MSB.

31. A digital computing system comprising:

an arithmetic device to add a plurality of numbers in redundant form;

bypass circuitry to bypass a result in a redundant form as input to the arithmetic device;

a receiving circuit to receive the result from the bypass circuitry and to generate a complemented redundant form of at least one number supplied to the arithmetic device;

a control unit to direct an adjustment input to the arithmetic device to adjust a result produced by adding to generate an outcome of a subtraction operation represented in a redundant form; and

a magnitude comparison logic coupled with the arithmetic device to generate a comparison result indicating the truth of a magnitude comparison of said at least one number to at least one other number of the plurality of numbers in redundant form.